

## REMARKS

In the Office Action, the Examiner rejected claims 1, 18, and 28 under 35 USC §112 and rejected the claims under 35 USC §102 and 35 USC §103. These objections and rejections are fully traversed below. In addition, the Examiner stated that claims 8, 9, 15, 16, 25, and 26 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

The claims have been amended to correct minor informalities and to further clarify the subject matter regarded as the invention. In addition, claims 8, 9, 15, 16, 25, and 26 have been amended to include all of the limitations of the base claim and any intervening claims. New claims 34-35 directed to a single processor system have been added. Claims 1-35 are now pending.

Reconsideration of the application is respectfully requested based on the following remarks.

### REJECTION OF CLAIMS 1, 18, AND 28 UNDER 35 USC §112

In the Office Action, the Examiner rejected claims 1, 18, and 28 under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. The claims have been amended to correct the typographical error referenced by the Examiner. Hence, Applicant respectfully requests that the Examiner withdraw the rejection of claims 1, 18, and 28 under 35 USC §112, second paragraph.

### REJECTION OF CLAIMS 1-2, 6, 12-13, 22-23, AND 33 UNDER 35 USC §102

In the Office Action, the Examiner rejected claims 1-2, 6, 12-13, 22-23, and 33 under 35 USC §102 as being unpatentable over Torii, U.S. Patent No. 5,913,059, ('Torii' hereinafter). This rejection is fully traversed below

Torii discloses a multi-processor system for inheriting contents of a register from a parent thread to a child thread. See Title. Only data generated by an instruction prior to the thread generation instruction is inherited from the parent thread to a child thread. See abstract. Specifically, a multi-processor system has a plurality of processors. Each of the processors includes a register. When a thread generation instruction is issued from a first processor to a second processor, contents of the register of the first processor is inherited to that of the second processor. See Summary. Thus, Torii's applications are limited to a multi-processor system.

In contrast, the present invention provides thread-local storage support. This support may be implemented in a programming language such as the Java™ programming language. The present invention may be implemented in a system including a single processor, as well as multiple processors.

Claim 1, as amended, recites: "A method for providing inheritable thread-local storage from a parent thread to a child thread, the method comprising:

for each thread-local variable, mapping each thread-local variable ~~thread~~ to a value;  
and

when a parent thread creates a child thread, automatically iterating over the parent thread's inheritable thread-local values to create the child thread's initial values of one or more thread-local variables." Torii fails to disclose a system or method for mapping a thread-local variable to a value or iterating over the parent thread's inheritable thread-local values to create the child thread's initial values of one or more thread-local variables. Torii merely discloses copying data from a register (data generated by an instruction prior to the thread generation instruction) associated with a first processor to a register of a second processor in a multiprocessor system. Torii fails to disclose the use of thread-local variables

in the manner claimed. Accordingly, Applicant respectfully submits that claim 1 is patentable over the cited art.

Claim 2, as amended, depends from claim 1, and further recites: “wherein the step of mapping comprises maintaining a map, associated with each thread object, that maps each thread-local variable to a value; and the step of iterating comprises iterating over the map such that inheritable thread-local values associated with the parent thread are used to create the initial values of the one or more thread-local variables of the child thread.” Torii fails to disclose or suggest using inheritable thread-local values associated with the parent thread to create the initial values of the one or more thread-local variables of the child thread.

Accordingly, Applicant respectfully submits that claim 1 is patentable over the cited art.

Claim 6, as amended, depends from claim 1, and further recites “wherein a child thread’s initial value of a thread-local variable is a copy of a corresponding parent thread’s value of a thread-local variable.” As described above, Torii fails to disclose or suggest copying a value of a thread-local variable of a parent thread to a child thread’s initial value of a thread-local variable. Accordingly, Applicant respectfully submits that claim 6 is patentable over the cited art.

Claim 12, as amended, recites “A method for providing automatic value inheritance when a parent thread creates a child thread, the method comprising:

associating, for each thread object of the parent thread, each thread-local variable with a value; and

automatically iterating over the inheritable thread-local values of the parent thread to create a child value of a thread-local variable of a child thread corresponding to each inheritable parent value of a thread-local variable of the parent thread, when a the child thread is created.” Torii fails to disclose or suggest iterating over the inheritable thread-local values of the parent thread to create a child value of a thread-local variable of a child thread

corresponding to each inheritable parent value of a thread-local variable of the parent thread, when the child thread is created. Specifically, the invention disclosed in Torii is only applicable to multi-processor systems in which contents of a register is copied from one processor to another. Accordingly, Applicant respectfully submits that claim 12 and corresponding computer-readable medium claim 22 are patentable over the cited art.

Claim 13 depends from claim 12, and is patentable for at least the same reasons. In addition, Torii fails to disclose copying an inheritable value of a thread-local variable from a parent thread to a child thread. Accordingly, Applicant respectfully submits that claim 13 and corresponding computer-readable medium claim 23 are allowable over the cited art.

Claim 33, as amended, recites “A method for providing automatic inheritance of parent thread-local values to a child thread upon child thread creation, wherein a parent thread is associated with the parent’s thread-local values, the method comprising:

determining the parent’s inheritable thread-local values associated with one or more thread-local variables of the parent thread; and

automatically initializing the child’s thread-local values of one or more thread-local variables of the child thread corresponding to the parent’s inheritable thread-local values associated with the one or more thread-local variables of the parent thread, upon child creation of the child thread, based on a predetermined child value method.” Torii neither discloses nor suggests determining inheritable thread-local values associated with one or more thread-local variables of the parent thread. In addition, as described above, Torii neither discloses nor suggests automatically initializing the child’s thread-local values of one or more thread-local variables of the child thread corresponding to the parent’s inheritable thread-local values associated with the one or more thread-local variables of the parent thread, upon creation of the child thread. Moreover, Torii fails to disclose or suggest

performing this initialization based upon a predetermined child value method. Accordingly, Applicant respectfully submits that claim 33 is patentable over the cited art.

### **REJECTION OF CLAIMS UNDER 35 USC §103**

In the Office Action, the Examiner rejected claims 3, 18-19, and 28-29 under 35 USC §103 as being unpatentable over Torii in view of Kim et al, U.S. Patent No. 6,553,531, ('Kim' hereinafter). This rejection is fully traversed below.

Kim discloses a method and apparatus for random stimulus generation. See title. Specifically, the disclosed invention adds capabilities to a Hardware Verification Language (HVL) which facilitate the generation of random test data. Sources of random numbers are easily produced by simply adding a randomness attribute to a variable declaration of a class definition. Such variables are called random variables. See Abstract.

The Examiner asserts that Kim discloses maintaining a linked list for each thread that links inheritable thread-local values associated with the thread, citing col. 13, line 21-col. 14 line 46. Kim disclose a chain of records, which is connected as a doubly linked list. See col. 13, lines 23-44. Each record contains variables and additional information. See col. 13, line 45-col. 14, line 45. However, Applicant respectfully submits that Kim fails to disclose maintaining a linked list for a thread that links inheritable thread-local values associated with the thread. Rather, Kim merely discloses a linked list of records, each of which includes multiple variables.

As described above, Torii fails to disclose the claimed invention. In addition, Kim fails to cure the deficiencies of the primary reference. Moreover, there fails to be a motivation to combine these references, since Kim fails to disclose a multi-threaded process. Accordingly, Applicant respectfully submits that claims 3, 18-19, and 28-29 are patentable over the cited references.

In the Office Action, the Examiner rejected claims 4-5, 10-11, 17, 21, 27, and 31 under 35 USC §103 as being unpatentable over Torii in view of Kim in view of De Pauw, U.S. Patent No. 6,370,684, ('De Pauw' hereinafter). This rejection is fully traversed below.

De Pauw does disclose a hash table. However, De Pauw fails to disclose the use of a hash table in the manner claimed. In addition, De Pauw fails to cure the deficiencies of Torii and Kim. Accordingly, Applicant respectfully submits that claims 4-5, 10-11, 17, 21, 27, and 31 are patentable over the cited art.

In the Office Action, the Examiner rejected claims 7, 14, 24, and 32 under 35 USC §103 as being unpatentable over Torii in view of Galloway, U.S. Patent No. 6,378,004, ('Galloway' hereinafter). This rejection is fully traversed below.

Galloway discloses a method of communicating a synchronous elements from a mini-port driver. See title. An lpThreadAttributes parameter is a pointer to a structure that determines whether the return handle can be inherited by a child process. The lpStart Address parameter points to the application-supplied function to be executed by the thread and represents the starting address of the thread. The lpParameter parameter specifies a single 32-bit parameter value for an argument for the new thread. See col. 6, lines 44-67.

Galloway fails to cure the deficiencies of the primary reference. Accordingly, Applicant respectfully submits that claims 7, 14, 14, 24, 24, and 32 are patentable over the cited art.

In the Office Action, the Examiner rejected claims 20 and 30 under 35 USC §103 as being unpatentable over Torii in view of Kim in view of Galloway. This rejection is fully traversed below.


Galloway fails to cure the deficiencies of Torii and Kim. Accordingly, Applicant respectfully submits that claims 20 and 30 are patentable over the cited art.

The additional limitations recited in the independent claims or the dependent claims are not further discussed as the above discussed limitations are clearly sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of the claims under 35 USC §102 and 35 USC §103(a).

If there are any issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for an extension of time which may be required to maintain the pendency of this case, and any required fee for such extension or any further fee required in connection with the filing of this Amendment is to be charged to Deposit Account No. 50-0388 (Order No. SUN1P247).

Respectfully submitted,  
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